REMARKS

Applicant respectfully requests the Examiner's reconsideration of the present application as amended.

Claims 1-55 are pending in the present application.

Claims 1-55 are rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent Application 2003/0051222 ("Williams").

Claims 1, 7, 33, 39, and 48 have been amended.

Support for amended claims 1, 7, 33, 39 and 48 is found on pages 4-28 of the specification, Figures 1-8(k) of the drawings, and claims 1-55 as originally filed. No new matter has been added.

The Examiner has rejected claims 1-55 under 35 U.S.C. §102(e) as being anticipated by Williams. In particular, the Examiner has stated that

> As to claims 1, and 33, Williams et al. teach a method for designing a system, comprising: determining minimum and maximum delay budgets for connections (see fig 6, 8-10, 11, and 12 paragraph 0055-0058 and paragraph 0061); and selecting routing resources for the connections in response to the minimum and maximum delay budgets (see fig 6, 8-10, 11 and 12 paragraph 0058-0065).
>
> . . .
>
> As to claims 7, and 39, Williams et al. teach wherein determining minimum and maximum delay budgets for the connections comprises finding a set of connection delays that attempt to satisfy the short-path and long-path timing constraints (see fig 11, fig 12 paragraph 0060-61).

(9/6/2005 Office Action, p. 2, and 3)

As stated above, claims 1, 7, 33, 39, and 48 have been amended.

It is submitted that Williams does not render claims 1-55, as amended, unpatentable under 35 U.S.C. §102(e).

Williams includes a disclosure of a method for designing an integrated circuit by adding sufficient margins early to allow a design to converge with only a handful of

iterations for each block type and for the top level. Delay calculations are based on worst-case values (See paragraphs [0030] and [0031]).

It is submitted that Williams does not teach or suggest determining minimum and maximum delay budgets for connections by finding a set of connection delays that satisfy short-path and long-path timing constraints, and selecting routing resources for the connections in response to the minimum and maximum delay budgets.

On the contrary, Williams discloses minimum and maximum boundaries that are used for modeling. The minimum and maximum boundaries are computed from physical and electrical device properties, and from manufacturing uncertainties. The additional margins are generated to account for the effects on timing of process spread, variations in dielectric thickness or permittivity, on-chip process tilt, on-chip variation in power-supply voltage drops, and inaccuracies in extraction and transistor characterizations (see Williams [0020-0021]). The minimum and maximum values in Williams are not determined from short-path and long-path timing constraints.

Furthermore, Williams discloses using the minimum and maximum boundaries for timing analysis, not for selecting routing resources. The minimum and maximum delays for every net is backannotated into timing analysis (see paragraph [0023]). The Examiner cites paragraphs [0058]-[0065] for support. Paragraphs [0058]-[0064] do not discuss routing. Paragraph [0065] only states the following.

> In the early stages of physical implementation, it is best to set high goals for both internal block timing and for the top-level timing (as judged by linearized signal velocity, discussed earlier). As a design progresses toward tapeout, and the top-level timing gets replaced with actual timing models derived from routed and timed blocks, the goals can be relaxed towards the eventual tapeout requirement target. Because gate-sizing changes, repeater insertion, and hold-element insertion all are "disruptions" in a routed design, they can have timing effects on neighboring objects (cell instances) or wires.

(Williams paragraph [0065]).

Applicants submit that Williams fails to disclose selecting routing resources for connections in response to the minimum maximum delay budgets.

In contrast, amended claim 1 as amended states

> A method for designing a system, comprising:
> determining minimum and maximum delay budgets for connections by finding a set of connection delays that satisfy short-path and long-path timing constraints; and
> selecting routing resources for the connections in response to the minimum and maximum delay budgets.

(Claim 1 as amended) (Emphasis added).

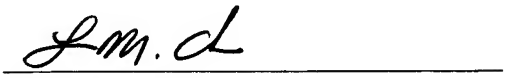
Claims 33, and 48, as amended, include similar limitations. Given that claims 2-32, 52-55, depend directly or indirectly from claim 1 as amended, claims 34-47 depend directly or indirectly from claim 33 as amended, and claims 49-51 depend directly or indirectly from claim 48 as amended, it is likewise submitted that claims 2-32, 34-47, and 49-55 are also patentable under 35 U.S.C. §102(e) over Williams.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-55, as amended, should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

Dated: December 6, 2005



Lawrence M. Cho
Attorney for Applicant
Registration No. 39,942

P.O. Box 2144
Champaign, IL 61825
(217) 377-2500